Jc715 U.S. PTO
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Subclass	ISSUE CLASSIFICATION
Class	

JC3/869

PATENT NUMBER

U.S. **UTILITY** Patent Application

O.I.P.E.	PATENT DATE
SCANNED KS(4) Q.A. VC	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/738485		~~327~~	226	~~2815~~ 2183	Harkness

APPLICANTS: Peter Korger

TITLE: Configurable hardware register stack for CPU architecture

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PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner)		_____ (Date)	NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	_____ (Primary Examiner)		_____ (Date)	ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.	_____ (Legal Instruments Examiner)		_____ (Date)	ISSUE BATCH NUMBER	

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